In the Claims:

Please amend the claims as follows:

1. (Currently Amended) A programmable circuit, comprising ~~operable to~~:

a programmable logic integrated circuit, the programmable logic integrated circuit including an interface operable to,

receive multiple versions of firmware from an external source, each version of firmware representing a corresponding operating configuration;

store the multiple versions of firmware in a memory; and

download a selected one of the versions of firmware from the memory.

2. (Previously Presented) The programmable circuit of claim 1, further operable to operate in the operating configuration corresponding to the downloaded version of firmware after downloading this version of firmware from the memory.

3. (Original) The programmable circuit of claim 1 wherein the memory comprises a nonvolatile memory.

4. (Currently Amended) The programmable circuit of claim 1 wherein the memory comprises ~~an external~~ memory external to the programmable logic integrated circuit.

5. (Currently Amended) A programmable circuit ~~operable to~~, comprising:

a programmable logic integrated circuit, the programmable logic integrated circuit including an interface operable to,

download from a memory storing a plurality of versions of firmware a first firmware version that represents a first configuration;

operate in the first configuration;

download from the memory a second firmware version that represents a second configuration; and

operate in the second configuration.

6. (Currently Amended) The programmable circuit of claim 5 wherein the programmable logic integrated circuit is further operable to:

receive the second firmware version from an external source while operating in the first configuration; and

storing the second firmware version in the memory while operating in the first configuration, and wherein the second firmware version may only be received when operating in the first configuration.

7. (Currently Amended) A programmable-circuit unit, comprising:

a memory; and

a programmable logic integrated circuit coupled to the memory, the programmable logic integrated circuit including an interface that is ~~and~~ operable to,

receive multiple versions of firmware from an external source, each version of firmware representing a corresponding operating configuration of the programmable circuit,

store each of the versions of firmware in the memory, and

download a selected one of the firmware versions from the memory.

8. (Original) The programmable-circuit unit of claim 7 wherein the memory comprises an electrically erasable and programmable read-only memory.

9. (Original) The programmable-circuit unit of claim 7 wherein the programmable circuit comprises a field-programmable gate array.

10. (Currently Amended) A programmable-circuit unit, comprising:

a memory operable to store a plurality of versions of firmware data, each version respectively representing a corresponding configuration of the programmable-circuit unit; and

a programmable logic integrated circuit coupled to the memory and including an interface that is operable to,

download a first selected one of the versions of firmware data from the memory,

operate in the configuration corresponding to the first selected version of firmware data,

download a second selected one of the versions of firmware data from the memory, and

operate in the configuration corresponding to the second selected version of firmware data.

11. (Currently Amended) The programmable-circuit unit of claim 10 wherein the programmable logic integrated circuit is further operable to:

receive the second selected version of firmware data from an external source while operating in the first configuration; and

store the second selected version of firmware data in the memory while operating in the first configuration, and wherein the second selected firmware version of firmware may only be received and stored when operating in the configuration corresponding to the first selected version of firmware data.

12. (Currently Amended) The programmable-circuit unit of claim 10 wherein the programmable logic integrated circuit is operable to load the second firmware while operating in the first configuration.

13. (Currently Amended) A programmable-circuit unit, comprising:

a memory operable to store a plurality of firmware configurations, each firmware configuration respectively representing a corresponding operational configuration;

a first programmable logic integrated circuit coupled to the memory and including an interface that is operable to,

download a first selected one of the firmware configurations from the memory,

operate in the operational configuration corresponding to the first selected firmware configuration,

download a first different one of the firmware configurations from the

memory, and

operate in the operational configuration corresponding to the first different firmware configuration; and

a second programmable logic integrated circuit coupled to the memory and to the first programmable circuit and including an interface that is operable to,

download a second selected one of the firmware configurations from the memory,

operate in the operational configuration corresponding to the second selected one of the firmware configurations,

download a second different one of the firmware configurations from the memory, and

operate in the operational configuration corresponding to the second different firmware configuration.

14. (Currently Amended) The programmable-circuit unit of claim 13 wherein the first programmable logic integrated circuit is further operable to:

receive the first and second different ones of the firmware configurations from an external source while operating in ~~the~~ a first configuration; and

store the first and second different ones of the firmware configurations in the memory while operating in the first configuration.

15. (Currently Amended) The programmable-circuit unit of claim 13 wherein the first and second programmable logic integrated circuits comprise respective field-programmable gate arrays.

16. (Currently Amended) A computing machine, comprising:

a processor;

an industry-standard bus coupled to the processor, the industry-standard bus adapted to be coupled to standard peripheral devices; and

~~a programmable-circuit unit coupled to the processor and comprising,~~

a memory that stores a plurality of firmware configurations ~~for the programmable-circuit unit,~~ ; and

a programmable logic integrated circuit coupled to the memory, and the programmable logic integrated circuit coupled to the processor through the industry-standard bus, the programmable integrated circuit operable to,

receive from the processor a new firmware configuration that represents a new configuration of the programmable circuit,

store the new firmware configuration in the memory, and

download the new firmware configuration from the memory in response to the processor.

17. (Currently Amended) The computing machine of claim 16 wherein the processor is operable to:

before sending the new firmware configuration to the programmable logic integrated circuit, determine whether the new firmware configuration is already stored in the memory; and

send the new firmware configuration to the programmable circuit only if the firmware is not already stored in the memory.

18. (Previously Presented) The computing machine of claim 16, further comprising:

a configuration registry coupled to the processor and operable to store the new firmware configuration and to indicate that the firmware configuration represents a desired configuration for the programmable circuit; and

wherein the processor is operable to download the firmware configuration from the configuration registry to the programmable circuit.

19. (Currently Amended) The computing machine of claim 16, wherein:

~~the programmable circuit unit comprises a pipeline unit; and~~

the programmable logic integrated circuit includes a hardwired pipeline that is operable to operate on data.

20. (Currently Amended) A computing machine, comprising:

a processor;

an industry-standard bus coupled to the processor, the industry-standard bus adapted to be coupled to standard peripheral devices; ~~and~~

~~programmable circuit unit coupled to the processor and comprising,~~

a memory operable to store a plurality of firmware versions that respectively represent configurations of ~~the~~ a programmable logic integrated circuit, ~~circuit unit; and a~~ the programmable logic integrated circuit being coupled to the memory and being coupled to the processor through the industry-standard bus, the programmable logic integrated circuit operable to,

download a selected one of the firmware versions from the memory,

operate in the configuration corresponding to the downloaded firmware version,

download a different firmware version from the memory in response to the processor, and

operate in the configuration corresponding to the different firmware version.

21. (Currently Amended) The computing machine of claim 20 wherein:

the processor comprises a first test port;

the programmable logic integrated circuit ~~circuit unit~~ comprises a second test port that is coupled to the first test port; and

the processor is operable to load the selected one of the firmware versions into memory via the first and second test ports.

22. (Currently Amended) The computing machine of claim 20 wherein:

the processor comprises a first test port;

the programmable ~~circuit unit~~ logic integrated circuit comprises a second test port that is coupled to the first test port;

while operating in the configuration corresponding to the selected one of the firmware versions, the programmable logic integrated circuit is operable to perform a self test and to provide self-test data to the processor via the first and second test ports; and

the processor is operable to cause the programmable logic integrated circuit to download the different firmware version from memory only if the self-test data indicates a predetermined result of the self test.

23. (Currently Amended) The computing machine of claim 20 wherein:

the processor is operable to send the selected one of the firmware versions to the programmable logic integrated circuit; and

while operating in the configuration corresponding to the selected one of the firmware versions, the programmable logic integrated circuit is operable to load the different firmware version into the memory in response to the processor.

24. (Currently Amended) A computing machine, comprising:

a processor;

an industry-standard bus coupled to the processor and adapted to be coupled to standard peripheral devices; ~~and~~

~~programmable circuit unit coupled to the processor and comprising,~~

a memory operable to store a plurality of firmware codes that respectively represent configurations,

a first programmable logic integrated circuit coupled to the memory and coupled to the processor through the industry-standard bus, the first programmable logic integrated circuit ~~and~~ operable to,

download ~~the~~ a first firmware code from the memory,

operate in a first configuration corresponding to the first firmware code,

download a second firmware code from the memory in response to the processor, and

operate in a second configuration corresponding to the second firmware code, and

a second programmable logic integrated circuit coupled to the memory and to the first programmable circuit, and coupled to the processor through the industry-standard bus, the second programmable logic integrated circuit ~~and~~ operable to,

download a third firmware code from the memory,

operate in a third configuration corresponding to the third firmware

code,

download a fourth firmware code from the memory in response to the processor, and

operate in a fourth configuration corresponding to the fourth ~~configuration~~ firmware code.

25. (Cancelled)

26. (Currently Amended) The computing machine of claim 24 wherein:

~~the processor comprises a first test port;~~

~~the programmable circuit unit comprises a second test port that is coupled to the first test port;~~

while operating in the first configuration, the first programmable logic integrated circuit is operable to perform a first self test and to provide first self-test data to the processor ~~via the first and second test ports~~;

while operating in the third configuration, the second programmable logic integrated circuit is operable to perform a second self test and to provide second self-test data to the processor ~~via the first and second test ports~~; and

the processor is operable to cause the first and second programmable circuits to respectively load the second and fourth firmware codes from the memory only if the first and second self-test data indicate respective predetermined results of the first and second self tests.

27. (Currently Amended) The computing machine of claim 24 wherein:

the processor is operable to send the second and fourth firmware codes to the first programmable logic integrated circuit; and

while operating in the first configuration, the first programmable logic integrated circuit is operable to load the second and fourth firmware codes into the memory in response to the processor.

28. (Currently Amended) The computing machine of claim 24 wherein the memory comprises:

a first memory section coupled to the first programmable logic integrated circuit and operable to store the first and second firmware codes; and

a second memory section coupled to the first and second programmable logic integrated circuits and operable to store the third and fourth firmware codes.

29. (Original) The computing machine of claim 28 wherein the first and second memory sections are respectively disposed on first and second integrated circuits.

30. (Currently Amended) A method, comprising:

providing a plurality of firmware codes directly to a programmable logic integrated circuit, each firmware code representing a configuration of the circuit;

storing each of the firmware codes in a memory with the programmable logic integrated circuit; and

downloading a selected one of the firmware codes from the memory ~~into~~ to configure the programmable logic integrated circuit.

31. (Original) The method of claim 30, further comprising operating in the configuration after downloading the configuration data from the memory.

32. (Currently Amended) A method, comprising:

storing in a memory a plurality of firmware codes, each firmware code representing a configuration of a programmable logic integrated circuit;

downloading over an industry-standard bus directly into the programmable logic integrated circuit a first firmware code that represents a first configuration;

operating the programmable logic integrated circuit in the first configuration;

downloading into the programmable logic integrated circuit second firmware that represents a second configuration; and

operating the programmable logic integrated circuit in the second configuration after downloading the second firmware.

33. (Currently Amended) The method of claim 32 wherein downloading the second firmware code comprises:

sending the second firmware code to the programmable logic integrated circuit;

loading the second firmware code into the memory with the programmable logic integrated circuit while the programmable logic integrated circuit is operating in the first configuration; and

downloading the second firmware code from the memory into the programmable logic integrated circuit.

34. (Currently Amended) The method of claim 32 wherein downloading the second firmware code comprises:

determining whether the second firmware code is stored in the memory coupled to the programmable logic integrated circuit;

sending the second firmware code to the programmable logic integrated circuit only if the second firmware code is not stored in the memory;

loading the second firmware code into the memory with the programmable logic integrated circuit while the programmable logic integrated circuit is operating in the first configuration; and

downloading the second firmware code from the memory into the programmable logic integrated circuit.

35. (Currently Amended) The method of claim 32 wherein:

operating the programmable logic integrated circuit in the first configuration comprises testing the programmable logic integrated circuit; and

downloading the second firmware code comprises downloading the second firmware code only if the programmable logic integrated circuit passes the testing.

36. (Currently Amended) A method, comprising:

storing in memory a plurality of firmware codes, each firmware code defining a corresponding operational configuration for one of first and a second programmable logic integrated circuit;

downloading over an industry-standard bus a first and a second one of the firmware codes into the first and second programmable logic integrated circuits, respectively;

operating the first and second programmable logic integrated circuits in the first and

second operational configurations, respectively;

downloading a third and a fourth firmware code into the first and second programmable logic integrated circuits, respectively, via the first programmable logic integrated circuit; and

operating the first and second programmable logic integrated circuits in the third configuration and fourth configurations, respectively.

37. (Cancelled)

38. (Currently Amended) The method of claim 36 wherein:

operating the first and second programmable logic integrated circuits in the first and second configurations comprises testing the first and second programmable logic integrated circuits; and

loading the third and fourth firmware codes into the first and second programmable logic integrated circuits comprises,

loading the third firmware code only if the testing indicates that the first programmable logic integrated circuit is functioning as desired, and

loading the fourth firmware code only if the testing indicates that the second programmable logic integrated circuit is functioning as desired.